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1.0 GENERAL

This manual provides the information necessary to install and operate the Model 6130A Panel Counter which is a Universal Digital Panel Counter designed to produce accurate digital indications of industrial measurements involving frequency or RPM. The Model 6130A Panel Counter provides a choice of two input circuits. The Isolated Input is a low level, optically-isolated circuit with a 1 megohm input impedance. It passes input frequencies over the range from dc to 100 kHz. The TTL Input circuit is a non-isolated input having a fan in one TTL unit load. This circuit will typically pass frequencies from dc to 10 MHz.

The counter has six basic modes in which it can operate (and several variations of each).

1. Frequency (External Input, Internal Gate).
2. Frequency Ratio F1/F2 (External Input, External Gate).
3. Time Interval (Internal Input, External Gate).
4. Period Average (Internal Input, External Gate).
5. Stop Watch (Internal Input, External Gate).
6. Totalize (External Input, External Gate).

Any one of thirteen gate periods, 1 us to 10 seconds or an external gate period may be selected by grounding an appropriate set of programming pins on the rear connector. See Table 1-1.

The prescaler can be used to divide either the counted signal or the Time Base by any integer from 2 to 12. Jumpers on the rear connector select the ratio. See Table 1-2. Frequency response is from dc to typically 10 MHz.

There is a provision for an external clock source when the internal crystal accuracy is not adequate (equivalent to RATIO mode).

The display consists of .56 inch, 7 segment LED display digits. Any decimal point to the right of the four most significant digits may be selected by a jumper on the lower connector J2. See Table 1-3.

A single LED annunciator located in the lower left-hand corner of the display provides visual overflow indication.

A front panel pushbutton switch is provided in the lower right hand area of the display. This switch (accessible at rear connector P2, pin P) can be wired to reset the internal counter and be used to initiate another measurement cycle at any time.

The architecture of this counter is in blocks of functional use, i.e. the input amplifiers, and control block, etc. are accessible via the rear connector pins and are wholly separate modules (except R1). DTL gated BCD outputs are available at the rear printed circuit connector. Outputs are gated with an enable line to allow common bussing with the BCD outputs of other instruments having this capability. Also, negative true outputs may be obtained by replacing the OR gates with pin compatible NAND gates.
1.1 GENERAL SPECIFICATIONS

Frequency Range
- Ac Input (Isolated) 1 Hz - 100 kHz
- Dc Input (Isolated) Dc - 100 kHz
- TTL Input Dc - 8 MHz min. 12 MHz typ.

Accuracy
See Mode Specifications

Gate Times
1 us to 10 seconds in decade steps and .001 min., .01 min., .001 hr., 100 s, 1 min., 1 hr., 10 min., and 20 ms. See Table 1-1.

Ext Gate Input
- TTL compatible

Capacity
99,999 counts

Display Storage
Store or non-store selectable by rear connector jumper.

Display Type
7-Segment LED

Display Size
.56" High Numerals

Decimal Points
Lower right of each digit (except LSD), jumper selectable.

Overflow Indicator
Single LED annunciator indicates count has exceeded internal counters capacity.

Signal Inputs

- Ac or dc Input (low level, isolated)

  Frequency Range 1 Hz or dc to 100 kHz.
  Delay 0 to 6 us with 50 mV peak input.
  Input Impedance 1 megohm with or without .1 uf in series.
  Coupling Ac or dc.
  Hysteresis 20 mV peak to peak, nominal.
  Sensitivity
    Sine Wave 1 20 mV RMS 5 Hz or dc to 20 kHz derated to 40 mV RMS at 1 Hz (ac) and 100 kHz.
    Square Wave 1 ±28 mV peak from average in ac, from ISO GND in dc, derated to 50 mV at 100 kHz.
  Trigger Error ±(2.5 mV + Peak Input Noise)/input slope.
  Maximum Input Voltage (from Iso. Gnd) 220 V RMS (+200 V Blocking in ac)
  Isolation Voltage 350 V peak (ISO GND to GND)
  Output Drive 19 LP-TTL unit loads

1 NOTE: The region between -28 mV and +28 mV dc is not defined.
TTL Input

- Frequency Range: Dc to 8 MHz min. Dc to 12 MHz typical
- (50% Duty Factor)
- Delay: 0 to 150 ns
- Coupling: Dc
- Sensitivity: Approximately 1 TTL unit load
- Trigger Error: ±.1 V/input slope
- Output Drive: 19 LP-TTL unit loads
- Time Base Accuracy: 2 x 10^{-6}/mo.; 2 x 10^{-6}/°C
- Optional: 3 x 10^{-7}/mo.; 2 x 10^{-7}/°C
- Divider Delay (internal clock): 0 to 4 us (varies by 1 us for fixed divider ratio)
- Operating Temperature: 0°C to 50°C
- Predivider: Externally programmable for integers 2,3,4,5,6,7,8,9,10,11,12.
- Power: 115/230 V ac ±10% 50-60 Hz, 10 watts max.
- Overall Dimensions: 48 mm High x 96 mm Wide x 141.5 mm Deep. (1.93 in x 3.82 in x 5.40 in)

1.2 MODE SPECIFICATIONS

Period Average Mode

- Full Scale: .99999 us to 99999 us
- Measurement Time: 99999 us (.1s) at Full Scale
- Accuracy: ±1 count ±Time Base Accuracy ±Trigger Error

Period and Time Interval Modes

- Full Scale: 99.999 ms to 999,990 seconds
- Measurement Time: Same as reading (excluding overhead time of 50 us).
- Accuracy: (Input circuit delay to STOP) -(Input circuit delay to START) - Divider Delay ±1/2 count ± Time Base Accuracy ± Trigger Errors
Frequency Ratio Mode

Display KF1/F2
K (divider ratio) See Table 1-1.
F1 Frequency See input circuit characteristics above.
F2 Frequency Dc to 1 MHz
Accuracy ±1/2 to 1 count (of F1)
± Trigger Error (of F2)

NOTE: For F1/F2 much less than 1, the synchronous Time Base reduces the normal ±1 count to a ±1/2 count roundoff.

Frequency Mode

Full Scale 9999.9 Hz to 999.99 kHz without prescaler.
Measurement Time 0.1 s to 10 s (Faster readings are possible to lesser resolution).
Accuracy ±1/2 to 1 count ± Time Base Accuracy ± Trigger Error

NOTE: For Input Frequency much less than 1 MHz, the synchronous Time Base reduces the normal ±1 count to a ±1/2 count roundoff.

Stop Watch Mode

Full Scale 99999 ms to 999,990 s (Manual switching makes shorter time scales meaningless)
Accuracy ±1/2 count ± Time Base Accuracy

Totalize Mode

Event Rate Dc to 2 MHz (TTL Input)
Accuracy Absolute provided CNT is low when ENB2 goes high.

1.3 SCALE SELECTION TABLES

Tables 1-1 through 1-3 give the connections to be made for selecting Time Base (or Divider Ratio), Predivider Ratio, and Decimal Location respectively.
Table 1-1. Time Base Selection

The Time Base (or Divider Ratio) is programmed by grounding or opening the time base TB1, 2, 4, 8 inputs per the following table:

<table>
<thead>
<tr>
<th>-TB-</th>
<th>DIVIDES BY (EXT OR INT)</th>
<th>TIME BASE (INT)</th>
</tr>
</thead>
<tbody>
<tr>
<td>8 4 2 1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0 0 0 0</td>
<td>$10^0$</td>
<td>1 us</td>
</tr>
<tr>
<td>0 0 0 1</td>
<td>$10^1$</td>
<td>10 us</td>
</tr>
<tr>
<td>0 0 1 0</td>
<td>$10^2$</td>
<td>100 us</td>
</tr>
<tr>
<td>0 0 1 1</td>
<td>$10^3$</td>
<td>1 ms</td>
</tr>
<tr>
<td>0 1 0 0</td>
<td>$10^4$</td>
<td>10 ms</td>
</tr>
<tr>
<td>0 1 0 1</td>
<td>$10^5$</td>
<td>100 ms</td>
</tr>
<tr>
<td>0 1 1 0</td>
<td>$10^6$</td>
<td>1 s</td>
</tr>
<tr>
<td>0 1 1 1</td>
<td>$10^7$</td>
<td>10 s</td>
</tr>
<tr>
<td>1 0 0 0</td>
<td>$10^5 (10^8)$</td>
<td>100 ms (100 s)</td>
</tr>
<tr>
<td>1 0 0 1</td>
<td>$6 \times 10^4 (6 \times 10^7)$</td>
<td>$10^{-3}$ min. (1 min.)</td>
</tr>
<tr>
<td>1 0 1 0</td>
<td>$36 \times 10^5 (36 \times 10^8)$</td>
<td>$10^{-3}$ hr. (1 hr.)</td>
</tr>
<tr>
<td>1 0 1 1</td>
<td>$6 \times 10^5 (6 \times 10^8)$</td>
<td>$10^{-2}$ min. (10 min.)</td>
</tr>
<tr>
<td>1 1 1 0</td>
<td>$2 \times 10^4$</td>
<td>20 ms</td>
</tr>
</tbody>
</table>

NOTE: 0 = Ground  
       1 = Open Input

The numbers in parentheses may be obtained by changing an internal jumper. Remove solder jumper A and install solder jumper B on Control Board.
Table 1-2. Predivider Selection

The Programmable Predivider may be used to divide either the counted signal or the Time Base by any integer from 2 to 12 by connecting P0 to P3 to open or ground per the following table:

<table>
<thead>
<tr>
<th>P3</th>
<th>P2</th>
<th>P1</th>
<th>P0</th>
<th>DIVISION RATIO</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>2</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>3</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>4</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>5</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>6</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>7</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>8</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>9</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>10</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>11</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>12</td>
</tr>
</tbody>
</table>

0 = Ground
1 = Open

NOTE:
6130As manufactured after mid-1987 will not divide by 11 or 12.

Table 1-3. Decimal Selection

The decimal selection is made by tying the decimal point common jumper from pin R to either pin 14, 15, 16, or 17 on the lower connector, J2.

<table>
<thead>
<tr>
<th>TERMINAL</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>J2-R</td>
<td>Decimal Point Common</td>
</tr>
<tr>
<td>J2-14</td>
<td>XXXX.X</td>
</tr>
<tr>
<td>J2-15</td>
<td>XXX.XX</td>
</tr>
<tr>
<td>J2-16</td>
<td>XX.XXX</td>
</tr>
<tr>
<td>J2-17</td>
<td>X.XXXX</td>
</tr>
</tbody>
</table>
### 1.4 PIN ASSIGNMENTS

**UPPER CONNECTOR J1**

<table>
<thead>
<tr>
<th>PIN NO.</th>
<th>NAME</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>SPRQ</td>
<td>Spare Flip-flop Q Output</td>
</tr>
<tr>
<td>B</td>
<td>SPRQ</td>
<td>Spare Flip-flop $\overline{Q}$ Output</td>
</tr>
<tr>
<td>C</td>
<td>SPRR</td>
<td>Spare Flip-flop Reset Input</td>
</tr>
<tr>
<td>D</td>
<td>SPRC</td>
<td>Spare Flip-flop Clock Input</td>
</tr>
<tr>
<td>E</td>
<td>REL</td>
<td>Release Input</td>
</tr>
<tr>
<td>F</td>
<td>GND</td>
<td>Digital Ground</td>
</tr>
<tr>
<td>H</td>
<td>GND</td>
<td>Digital Ground</td>
</tr>
<tr>
<td>J</td>
<td>PDO</td>
<td>Predivider Output</td>
</tr>
<tr>
<td>K</td>
<td>FOUR</td>
<td>Predivider FOUR Output</td>
</tr>
<tr>
<td>L</td>
<td>PDI</td>
<td>Predivider Input</td>
</tr>
<tr>
<td>M</td>
<td>PO</td>
<td>Predivider Select</td>
</tr>
<tr>
<td>N</td>
<td>P1</td>
<td>Predivider Select</td>
</tr>
<tr>
<td>P</td>
<td>P2</td>
<td>Predivider Select</td>
</tr>
<tr>
<td>R</td>
<td>P3</td>
<td>Predivider Select</td>
</tr>
<tr>
<td>S</td>
<td>EXT</td>
<td>External/Internal Time Base Select</td>
</tr>
<tr>
<td>T</td>
<td></td>
<td>+5 V through 100 ohms</td>
</tr>
<tr>
<td>U</td>
<td>TTL+</td>
<td>TTL Positive Output</td>
</tr>
<tr>
<td>V</td>
<td>ISO+</td>
<td>Isolated Positive Output</td>
</tr>
</tbody>
</table>

Key between pins 12 (N) and 13 (P).
### UPPER CONNECTOR J1

<table>
<thead>
<tr>
<th>PIN NO.</th>
<th>NAME</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>R2</td>
<td>Reset from Control</td>
</tr>
<tr>
<td>2</td>
<td>ENB1</td>
<td>Enable from Control</td>
</tr>
<tr>
<td>3</td>
<td>STOP</td>
<td>Stop Input</td>
</tr>
<tr>
<td>4</td>
<td>START</td>
<td>Start Input</td>
</tr>
<tr>
<td>5</td>
<td>GND</td>
<td>Digital Ground</td>
</tr>
<tr>
<td>6</td>
<td>HOLD</td>
<td>Hold Input</td>
</tr>
<tr>
<td>7</td>
<td>RESET</td>
<td>Reset Input</td>
</tr>
<tr>
<td>8</td>
<td>STRI</td>
<td>Strobe Output</td>
</tr>
<tr>
<td>9</td>
<td>XO</td>
<td>Crystal Output (1 MHz)</td>
</tr>
<tr>
<td>10</td>
<td>TB1</td>
<td>$2^0$ Time Base Input</td>
</tr>
<tr>
<td>11</td>
<td>TB2</td>
<td>$2^1$ Time Base Input</td>
</tr>
<tr>
<td>12</td>
<td>TB4</td>
<td>$2^2$ Time Base Input</td>
</tr>
<tr>
<td>13</td>
<td>TB8</td>
<td>$2^3$ Time Base Input</td>
</tr>
<tr>
<td>14</td>
<td>TBDO</td>
<td>Time Base Divider Output</td>
</tr>
<tr>
<td>15</td>
<td>TBDI</td>
<td>Time Base Divider Input</td>
</tr>
<tr>
<td>16</td>
<td>TTLIN</td>
<td>TTL Input</td>
</tr>
<tr>
<td>17</td>
<td>TTL-</td>
<td>TTL Negative Output</td>
</tr>
<tr>
<td>18</td>
<td>ISO</td>
<td>Isolated Negative Output</td>
</tr>
</tbody>
</table>

### BARRIER STRIP TB1

<table>
<thead>
<tr>
<th>PIN NO.</th>
<th>NAME</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>AC HI</td>
<td>Primary High Input</td>
</tr>
<tr>
<td>2</td>
<td>AC LO</td>
<td>Primary Low Input</td>
</tr>
<tr>
<td>3</td>
<td>AC GND</td>
<td>Primary Shield</td>
</tr>
<tr>
<td>4</td>
<td>ISO GND</td>
<td>Isolated Ground Input</td>
</tr>
<tr>
<td>5</td>
<td>ISO AC</td>
<td>Isolated ac Input</td>
</tr>
<tr>
<td>6</td>
<td>ISO DC</td>
<td>Isolated dc Input</td>
</tr>
<tr>
<td>PIN NO.</td>
<td>NAME</td>
<td>FUNCTION</td>
</tr>
<tr>
<td>--------</td>
<td>----------</td>
<td>---------------------------</td>
</tr>
<tr>
<td>A</td>
<td>1 BIT</td>
<td></td>
</tr>
<tr>
<td>B</td>
<td>2 BIT</td>
<td></td>
</tr>
<tr>
<td>C</td>
<td>4 BIT</td>
<td></td>
</tr>
<tr>
<td>D</td>
<td>8 BIT</td>
<td></td>
</tr>
<tr>
<td>E</td>
<td>100 BIT</td>
<td>BCD OUTPUTS</td>
</tr>
<tr>
<td>F</td>
<td>200 BIT</td>
<td>High true outputs. All</td>
</tr>
<tr>
<td>H</td>
<td>400 BIT</td>
<td>outputs high true when</td>
</tr>
<tr>
<td>J</td>
<td>800 BIT</td>
<td>disabled.</td>
</tr>
<tr>
<td>K</td>
<td>10 K BIT</td>
<td></td>
</tr>
<tr>
<td>L</td>
<td>20 K BIT</td>
<td></td>
</tr>
<tr>
<td>M</td>
<td>40 K BIT</td>
<td></td>
</tr>
<tr>
<td>N</td>
<td>80 K BIT</td>
<td></td>
</tr>
<tr>
<td>P</td>
<td>SW</td>
<td>Pushbutton Switch Output</td>
</tr>
<tr>
<td>R</td>
<td>DP1</td>
<td>Decimal Point Common</td>
</tr>
<tr>
<td>S</td>
<td>R3</td>
<td>Counter Chain Reset Input</td>
</tr>
<tr>
<td>T</td>
<td>OVF</td>
<td>Non-Stored Overflow Output</td>
</tr>
<tr>
<td>U</td>
<td>OVF1</td>
<td>Overflow Indicator Input</td>
</tr>
<tr>
<td>V</td>
<td>OVF5</td>
<td>Stored Overflow Output</td>
</tr>
</tbody>
</table>

Key between pins 4 (D) and 5 (E).
### LOWER CONNECTOR J2

<table>
<thead>
<tr>
<th>PIN NO.</th>
<th>NAME</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>STR2</td>
<td>Strobe Input</td>
</tr>
<tr>
<td>2</td>
<td>10 BIT</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>20 BIT</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>40 BIT</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>80 BIT</td>
<td>BCD OUTPUTS</td>
</tr>
<tr>
<td>6</td>
<td>1 K BIT</td>
<td>High true outputs. All outputs high true when disabled.</td>
</tr>
<tr>
<td>7</td>
<td>2 K BIT</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>4 K BIT</td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>8 K BIT</td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>RDY</td>
<td>Ready Output</td>
</tr>
<tr>
<td>11</td>
<td>ENB2</td>
<td>Counter Chain Enable Input</td>
</tr>
<tr>
<td>12</td>
<td>CNT</td>
<td>Counter Chain Input</td>
</tr>
<tr>
<td>13</td>
<td>OVFG</td>
<td>Gated Overflow Output</td>
</tr>
<tr>
<td>14</td>
<td>DP2</td>
<td>Decimal Point 2</td>
</tr>
<tr>
<td>15</td>
<td>DP3</td>
<td>Decimal Point 3</td>
</tr>
<tr>
<td>16</td>
<td>DP4</td>
<td>Decimal Point 4</td>
</tr>
<tr>
<td>17</td>
<td>DP5</td>
<td>Decimal Point 5</td>
</tr>
<tr>
<td>18</td>
<td>DIS</td>
<td>BCD Disable</td>
</tr>
</tbody>
</table>

### DECIMAL POINT CONNECTIONS

<table>
<thead>
<tr>
<th>PIN NO.</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>J2-R</td>
<td>Decimal Point Common</td>
</tr>
<tr>
<td>J2-14</td>
<td>XXX.X Decimal Point 2</td>
</tr>
<tr>
<td>J2-15</td>
<td>XXX.XX Decimal Point 3</td>
</tr>
<tr>
<td>J2-16</td>
<td>XX.XXX Decimal Point 4</td>
</tr>
<tr>
<td>J2-17</td>
<td>X.XXXX Decimal Point 5</td>
</tr>
</tbody>
</table>
2.0 RECEIVING AND INSTALLATION

2.1 UNPACKING AND INSPECTION

Your Model 6130A Universal Panel Counter has been carefully inspected and tested before shipment. Unpack the meter and perform a visual inspection to assure that no damage has occurred during shipment or handling. These meters are factory sealed units. The only controls that normally require periodic adjustment are accessible through the side panel. Because extensive damage could result from attempts to measure circuit parameters or to trouble-shoot the meter by non-factory personnel, the warranty is voided if the unit has been removed from its case and shows signs of unauthorized repair.

NOTE

No attempt should be made to operate this counter without first reading Section 3, since it is a Universal Panel Counter and requires several external interconnections to make it operate.

2.2 INSTALLATION - MECHANICAL

See page 37 for installation and mounting drawing. The unit is inserted in the front of the panel with slide retainers removed. Slide retainers are then installed from the rear and held in place by the clamp rings as shown in the diagram.

3.0 OPERATING INSTRUCTIONS

The 6130A Counter is capable of operating in several different modes. Six of the more common modes are presented here, however, other modes are possible which may better suit the user's requirements. Familiarity with the material presented should enable the user to select the connections required for his application.

Each mode requires both a signal to be counted and a gate signal. Several choices exist for the sources of these signals. The block diagram shown in Figure 3-1 shows the various circuits and the connections available that allow the counter to be connected in the different modes. These connections are made with jumpers on the rear panel connectors.

This section defines the functional blocks, explains the function of each input/output connection and gives the required connections to produce a properly functioning counter in each of the six modes presented.
FIGURE 3-1  BLOCK DIAGRAM
3.1 DESCRIPTION OF BLOCKS

3.1.1 Counter Block

The Counter Block includes the count gate with inputs CNT and ENB2, the 5 decade counter with reset input, R3, the latch-decoder-drivers, the displays and the output buffers with disable input, DIS, and the BCD outputs from all 5 digits plus overscale.

Counting is normally started when reset, R3, is taken high (ENB2 is already high) and stopped when ENB2 is taken low. This prevents false counts on START or STOP (if CNT is high). However, in TOTALIZE mode and some special cases, enabling can be done with ENB2 only.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Capacity</td>
<td>99999 counts</td>
</tr>
<tr>
<td>Count Rate</td>
<td>0 to 2 MHz</td>
</tr>
<tr>
<td>CNT</td>
<td>Count input, requires 250 ns minimum pulse width, high and low, triggers counter on positive edge. 2.2 LP-TTL unit loads.</td>
</tr>
<tr>
<td>ENB2</td>
<td>Enables the count gate when high. 4.4 LP-TTL unit loads.</td>
</tr>
<tr>
<td>R3</td>
<td>Resets (and holds reset) the counter when low. 5 LP-TTL unit loads.</td>
</tr>
<tr>
<td>STR2</td>
<td>Strobes data into the latch-decoder-drivers when low. 13.5 LP-TTL unit loads. Connection to GND makes display track counter continuously.</td>
</tr>
<tr>
<td>DIS</td>
<td>Disables output buffers when high. (Outputs go high) 3 TTL unit loads. (DTL OR'S)</td>
</tr>
<tr>
<td>BCD OUTPUTS</td>
<td>Active high 7.5 TTL unit loads drive. (DTL OR'S)</td>
</tr>
</tbody>
</table>
3.1.2 Control Block

The Control Block receives input signals REL, START, STOP, HOLD and RESET, and generates outputs R1, R2, ENB1, STRI, and RDY. When STOP receives a falling edge, strobe pulses are generated on STRI and RDY after which a reset is generated (provided HOLD is low) which sets R1 and ENB1 high and R2 low. R1 sets the TimeBase Divider to its maximum count state. R2 is normally tied to R3 and resets the counters. ENB1 is normally tied to ENB2 and enables the count gate. A falling edge on REL will remove the reset to the Time Base Divider, R1, and a falling edge on START will set R2 high and allow counting to start. This routine synchronizes the time base to the input signal within 1 us (+ a constant delay) which minimizes display bounce in many applications.

REL

Triggers a flip-flop on a negative edge which sets R1 low and releases the Time Base Divider. Two LP-TTL unit loads.

START

Triggers a flip-flop on a negative edge which sets R2 high. Two LP-TTL unit loads.

STOP

Triggers a flip-flop on a negative edge, provided R2 is high, sets ENB1 low and generates STRI and RDY. Two LP-TTL unit loads.

HOLD

Prevents resetting the control flip-flops when high. Sequence stops with RDY high and STRI high and holds data static. Allows sequence to proceed with low state or pulse to low for 200 ns minimum. May go high up to 15 us after RDY goes high and still catch that reading. 2.2 LP-TTL unit loads.

RESET

Causes Control flip-flops to reset when low for at least 20 us provided HOLD is low. Requires bounce-free rising edge. 2.2 LP-TTL unit loads.

R1

Generated from REL. This internally tied signal goes to RMAX of the Time Base Divider. When it goes low it releases the Time Base Divider and allows it to start dividing on the next oscillator pulse.

R2

Generated from START, this signal is normally tied to R3. When it goes low it resets the counter chain, its rising edge allows the counter to start counting. 19 LP-TTL unit loads drive.
ENB1

Normally tied to ENB2 to enable the count gate. Falling edge stops count. 20 LP-TTL unit loads drive.

ROD

Goes high for 20 us min. to indicate data is ready. 22 LP-TTL unit loads drive. (On Counter Board).

STR1

 Normally tied to STR2. This signal strobes data into the display latches. 22 LP-TTL unit loads drive.
3.1.3 Oscillator/Divider Block

The Oscillator/Divider Block includes a 1 MHz crystal controlled oscillator and a Time Base Divider which can be driven by the oscillator or by an external input, TBDI, and produces an output, TBDO, which is divided by \(10^N\) where \(N\) is any integer from 0 to 7 or by \(6 \times 10^4\) or \(6 \times 10^5\) or \(36 \times 10^5\).* The division factor and the external/internal control are accomplished by jumpers to GND on 5 control lines at the top connector (J2). The oscillator also provides a 1 MHz output, XO, that may be used to count microseconds for the Period Average Mode. R1 from the Control Block, when high, sets the Time Base Divider to its maximum state so that its output generates a negative edge on the first clock after the falling edge of R1.

- **R1**
  Internally tied signal. Resets Time Base Divider to its maximum state when high.

- **TBDI**
  Input to Time Base Divider. Enabled by a high on EXT. One TTL unit load dc to 1 MHz frequency response.

- **TBDO**
  Output from the Time Base Divider which is normally tied to START and STOP or CNT for various modes. This signal has a 50% duty cycle, resets to a high level and goes to a low level on the first clock after the falling edge of R1. 1 TTL unit load drive.

- **XO**
  1 MHz clock for connection to CNT in Period Average Mode. 4.5 LP-TTL unit loads drive.

- **EXT**
  This input controls the Time Base Divider frequency source. When at zero it selects the internal crystal source, when high it selects the external input, TBDI.

- **TB1, 2, 4, 8**
  Controls Time Base Divider Ratio. See Table 1-1.

*Additional divider ratios are available by changing an internal jumper. See Table 1-1.
3.1.4 Isolated Input Block

This input circuit is isolated from the rest of the counter via an optical isolator allowing up to 400 V peak from ISOGND to the meters system GND. The floating inputs ISOAC and ISODC are active with respect to ISOGND and drive a CMOS-Bipolar amplifier which drives the LED of the optical isolator. The receiving phototransistor of the isolator in turn drives another CMOS-Bipolar amplifier which is shaped by two logic buffers, generating ISO+ and ISO-.

**ISODC**
Isolated dc input. Maximum input is 240 V dc + peak ac. This is an alternate input to ISOAC, not a separate channel.

**ISOAC**
Isolated ac input. Up to 220 V RMS from ISOGND can be put on this input without damage. Dc blocking is up to ±200 V less ac peak signal.

**ISOGND**
This is the input return, which is floating with respect to the system ground, GND. The maximum voltage between these grounds is 350 V peak.

**ISO+**
This is a non-inverted TTL output signal and is 19 LP-TTL unit load drive with respect to GND.

**ISO-**
This is an inverted TTL output signal and is 19 LP-TTL unit loads drive with respect to GND.

3.1.5 TTL Input Block

The TTL Input circuit has a resistor-diode protection circuit followed by two inverters to allow for inputs which exceed the standard range of +5 V to 0 V without damage to the circuit. It is recommended that this circuit be used to buffer the input in most cases where the Isolated Input is not used.

**TTLIN**
TTL compatible input. Approximately 1 TTL unit load. Swing may go from +100 V to -20 V max.

**TTL+**
This is the non-inverted output signal. 19 LP-TTL unit loads drive.

**TTL-**
This is the inverted output signal. 19 LP-TTL unit loads drive.
3.1.6 Programmable Prescaler Block

The Programmable Prescaler may be used to divide either the counted signal, TTL+ or TTL-, or ISO+ or ISO-, or the Time Base output, TBDO, by any integer from 2 to 12. Four jumpers P0 to P3, are jumpered to GND to select the division ratio. The input is Prescaler Divider In, PDI, and the outputs are PDO and FOUR. PDO pulse s low for a time equal to the period of the input. FOUR gives a wider output pulse for divisions between 4 and 20 inclusive, which allows use of the prescaler for higher frequency inputs.

- **PDI**: Prescaler Divider Input. Requires 25 ns minimum pulse widths. 4.5 LP-TTL unit loads.
- **PDO**: Prescaler Divider Output. 17 LP-TTL unit loads drive.
- **FOUR**: This is the 4 bit output terminal of the divider. 17 LP-TTL unit loads drive.
- **P0,1,2,3**: Controls divider ratio. See Table 1-2.

3.1.7 Miscellaneous Units

There is a spare flip-flop that may be used to debounce a mechanical switch. It clocks to the set state on a falling edge at SPRC and resets on a low level at SPRR. The Q and Q outputs are at SPRQ and SPRQ respectively. (This flip-flop can be modified into a & 2 by removal of an internal jumper).

- **SPRC**: Spare flip-flop clock input
- **SPRR**: Reset line of spare flip-flop.
- **NOTE**: The spare flip-flop may be reset by spurious pulses. Connect SPRR to J1-T or add a 10 k resistor to +5 V.
- **SPRQ**: True output of spare flip-flop.
- **SPRQ**: False output of spare flip-flop.

Frequency response as a & 2 is 2.5 MHz.

A front panel pushbutton switch in the lower right hand area of the display provides a contact closure to GND at SW (rear connector P2 pin P) when depressed. When not depressed SW is pulled up by a 10 k resistor to +5 V.
3.2 EXTERNAL CONNECTIONS

3.2.1 Power

This counter operates from a 115/230 V ±10%, 50-60 Hz power source. It should be connected to the power source by a three-conductor cable as shown below for either 115 V operation or 230 V operation, whichever is supplied.

115/230 Volt Operation

Operation for 115 or 230 volts is determined by an internal jumper per customer order.

3.2.2 Signal Inputs

3.2.2.1 Isolated Signal - AC Input

This is a low level, high impedance isolated input. The input signal lead should be as short as possible and shielded to minimize external noise pickup. This input has 20 mV RMS sensitivity for sine wave inputs. For pulse inputs, sensitivity is ±28 mV peak from average. With a peak to peak signal of E and a duty factor of A ≤ 1/2, the peak value is EA ≥ 28 mV.

Isolated Signal - DC Input

This is an alternate input feed in through a 10 k resistor instead of the 0.1 uF capacitor. On special order, this resistor may be made higher to form an attenuator.

AC or DC Input Signal

Connection should be made as shown below:
3.2.2.2 TTL Input

The TTL logic input fan in is one TTL load. Connection should be made as shown below:

![TTL Signal Source Diagram]

NOTE: The TTL logic input is diode decoupled to withstand +24 V logic.

3.2.3 External Control Signals

3.2.3.1 Logic Levels - The control signals specified in terms of TTL or LP-TTL unit loads are as listed below. Mnemonic signal names written as FUNCTION are active low signals while all others are active high signals except for the BCD outputs which are active high with the standard OR output gates and active low with the optional NAND output gates.

Input Levels for TTL
- High 2.0 to 5.0 V
- Low 0 to 0.8 V

Output Levels for TTL
- High 2.4 to 5.0 V
- Low 0 to 0.4 V

Unit Load for TTL
- High 40 uA at 2.4 V (from output-to input)
- Low 1.6 mA at 0.4 V (from input-to output)

Input Levels for LPTTL
- High 2.0 to 5.0 V
- Low 0 to 0.7 V

Output Levels for LPTTL
- High 2.4 to 5.0 V
- Low 0 to 0.4 V

Unit Load for LPTTL
- High 10 uA at 2.4 V (from output-to input)
- Low 180 uA at 0.4 V (from input-to output)

3.2.3.2 Clock Output - The internal 1 MHz crystal oscillator output signal, XO, will drive 4.5 LPTTL unit loads. This is used for driving CNT in the Period Average mode, and PDIN for extension of the time base in various modes.
3.2.3.3 Time Base Divider Input - Normally this input is connected through the TIME BASE I.C. to the internal clock when the INTERNAL/EXTERNAL CLOCK SELECT is grounded by taking J1-S to ground on J1-F or H. The TIME BASE DIVIDER INPUT, TBDIN, is selected when pin S is open. This allows an external 1 MHz time base to be used when the supplied crystal signal is not sufficiently accurate. It is also used to divide the input for PERIOD AVERAGE or the "B" input for RATIO A/B.

3.2.3.4 Internal Gate times - The internal gate times are programmed by grounding or opening the time base TB1, 2, 4, 8 inputs per Table 1-1.

3.2.3.5 Store/Track - For the Store mode, tie STR2 (J2-1) to STR1 (J1-8). For the Track mode tie STR2 to GND and leave STR1 open. Also see paragraph 3.2.3.9 OVERFLOW.

3.2.3.6 Reset - To reset the counter during a measurement, ground RESET, J1-7. To use the front panel reset pushbutton connect SW (J2-P) to RESET (J1-7).

3.2.3.7 Programmable Predivider - The Programmable Predivider may be used to divide either the counted signal or the Time Base by any integer from 2 to 12 by connecting P0 to P3 to ground or left open as per Table 1-2.

The input signal is connected to the Predivider Input, PDI (J1-L) which can be from the Isolated Input amplifier, the TTL Input amplifier, or an external TTL signal with a 5 LPTTL unit load output drive capability. The FOUR output (J1-K) can only be used for division ratios of 4 to 10 inclusive since there is no output from this pin for ratios 2 and 3, and 2 pulses for 11 and 12. This output provides a wider output than does the Predivider Output. The Predivider Output, PDO (J1-J) is available for all division ratios but is only low for a period equal to the period of the input.

3.2.3.8 BCD Output Gates - The BCD Disable, DIS, on J2-18 is held low or a logic 0 to read the BCD data and held high to make the output go high. DIS requires 3 unit loads drive.

3.2.3.9 Overflow - The OVF output (J2-T) goes high when the counting capability of the display has been exceeded. The OVFG output (J2-13) goes high when the overflow (OVF) is high. The OVFS output goes high when OVF is high and data is stored. The OVFI input (J2-U) to the Overscale Indicator should be tied to OVFS (J2-V) for STORE operation or to OVF (J2-T) for Track operation.
3.2.3.10 Decimal Points - These control connections are on the bottom connector, J2. A jumper is soldered from the common terminal, DP1, to the selected decimal point terminal, DP2-5. DP2 corresponds to a decimal point on the right of the second least significant digit. See Table 1-3.

3.3 TYPICAL INTERCONNECTIONS

3.3.1 Frequency Mode - 10 MHz Full Scale

Refer to interconnection diagram Figure 3-2. This diagram shows how the TTL Input circuit and Predivider circuit are used for the high frequency (10 MHz) involved. Note that either TTL+ or TTL- may be used. The Predivider is connected for divide by ten and the Time Base divider for 100 ms gate time.

Once RESET time expires within the CONTROL BLOCK, the next negative edge of FOUR will remove R1 and release the Time Base Divider. The next clock will set the divider's output, TBDO, low which sets the START flip-flop, setting R2-high. This allows positive edges of FOUR to be counted until TBDO generates another negative edge - in this case 100 ms later - setting the STOP flip-flop which takes ENB1 low. This terminates the count, generates a strobe pulse on STR1 (stores data) and then resets the CONTROL BLOCK which resets the counter and the Time Base Divider. Reset within the CONTROL BLOCK expires approximately 50 ms after STOP allowing the next cycle to commence.
NOTE: POWER CONNECTIONS AND DECIMAL POINT JUMPERS NOT SHOWN.

FIGURE 3-2. FREQ. (999999 MHz F.S. - IPP ONLY) SYNCHRONOUS
NOTE: POWER CONNECTIONS AND DECIMAL POINT JUMPERS NOT SHOWN.

FIGURE 3.2A FREQ. (9.999MHz F.S. - TYP. ONLY)
ASYNCHRONOUS
This mode of operation may be described as semi-synchronous as an edge of the input signal enables the Time Base to start, but the clock itself is not syncable. The delay from the enabling edge of the input to the time when an edge may be counted can therefore vary by 1 us. This has the advantage of reducing display bounce for input frequencies less than 1 MHz at CNT (10 MHz at TTL for our example). For frequencies much less than 1 MHz (at CNT), the first count occurs one half cycle after the Time Base starts which gives a round off effect and reduces the phasing error (resolution) from ±1 count to ±1/2 count. (With predivider as shown it would be +.4 to -.6 count.)

The synchronous circuit of Figure 3.2 depends on the input signal to control the gate time of the counter. A characteristic of the synchronous circuit is that if the input signal is removed, the reading in the counter at the end of gate time will be held until another signal is applied. The circuit in Figure 3-2A will continue to sample with the input removed, and so will go to zero the first full gate time that no input has been present.

3.3.2 Frequency Ratio Mode
Refer to interconnection diagram, Figure 3-3. Note that this figure has some of the same interconnections as Figure 3-2. The differences are that the predivider is not used (which is optional in either case) and that external reference frequency, F2, is divided to generate the Time Base rather than the crystal oscillator. (EXT is not tied to GND and the divider takes its input from TBDI.) Otherwise, operation is the same as for Frequency Mode.

3.3.3 Period Average Mode
Refer to interconnection diagram, Figure 3-4. This diagram shows usage of the Isolated Input circuit to drive the Time Base Divider and the crystal oscillator output, XO, to count us. The Time Base Divider's output, TBD0, starts and stops the count with a period $10^N$ times that of the input. The input period averaged over $10^N$ cycles is therefore $R/10^N$us where R is the reading (total counts). Therefore, to display us with $N = 2$ as in our example, we select the decimal point for XXX.XX by jumpering DP1 to DP3.
NOTE: POWER CONNECTIONS AND DECIMAL POINT JUMPERS NOT SHOWN.

![Circuit Diagram](image)

**Figure 3-3** FREQUENCY RATIO \(10^5 \text{A/B-TYP ONLY}\)
NOTE: POWER CONNECTIONS AND DECIMAL POINT JUMPERS NOT SHOWN.

---

FIGURE 3-4. PERIOD AVERAGE (999.99,5 F.S.-TYP ONLY)
Operation proceeds much as in Frequency Mode above except that the roles of the input and the clock are reversed. REL, however, is still tied to the input circuit which simply enables the time base to start. No synchronous improvement is possible in this mode since the 1 us clock period (jitter) is worth 1 count.

3.3.4 Period Mode
Refer to interconnection diagram, Figure 3-5. This diagram shows how the edges of two different signals may be used to measure their time difference using both the Isolated Input Circuit and the TTL Input Circuit. Note that the delay through the TTL circuit is less than that through the lower speed Isolated Input Circuit so that, for short time increments, the reading will have an offset. This offset may be determined by tying both inputs to one signal and observing the reading.

Alternatively, one input circuit may be used to drive START and STOP to measure either pulse width (+) to START and (-) to STOP or vice versa) or period (either (+) or (-) to do both).

Operation is started by a negative edge on REL which removes the reset to the Time Base Divider. The next clock causes the Time Base Divider's output, TBDO, to go negative triggering START which removes the reset to the counter. This signal has a 50% duty factor so that the first positive edge, and the first count, occur one half cycle later.

For our example, we are counting milliseconds so the first count is after 1/2 ms giving a rounded off reading. Accuracy of round-off is limited by the dividers delay and the 1 us crystal clock period compared to the divided clock period (TBDO) so that better round off so obtained with longer time scales.

3.3.5 Stop Watch Mode
Refer to interconnection diagram Figure 3-6. This diagram shows how external switches may be used to count time. The Time Base Divider may be programmed for the desired resolution. The Reset and Start switch resets the counter to zero and starts the time count when pressed. Pressing the Stop switch halts the counter and holds the reading. The interconnection diagram 3-6A has separate START, STOP and RESET functions so that time can be accumulated.
NOTE: POWER CONNECTIONS AND DECIMAL POINT JUMPERS NOT SHOWN.

FIGURE 3-5: PERIOD A TO B (99.999 SEC. F.S. - TYP ONLY)
NOTE: POWER CONNECTIONS AND DECIMAL POINT JUMPERS NOT SHOWN.

Figure 3-6A: STOP WATCH - ACCUMULATE
9989.9 SEC. F.S.-TYP. ONLY
NOTE: POWER CONNECTIONS AND DECIMAL POINT JUMPERS NOT SHOWN.

FIGURE 3-7: TOTALIZE
3.3.6 **Totalize Mode**
Refer to interconnection diagram Figure 3-7. This diagram shows how the spare flip-flop may be used to condition a switch input. The Reset switch does not require debouncing provided it is released with the count stopped. Note also that RESET is independently controlled so that count may be restarted without resetting.

3.3.7 **Other Modes**
An interconnection blank is provided as Figure 3-8 for the users convenience.
NOTE: POWER CONNECTIONS AND DECIMAL POINT JUMPERS NOT SHOWN.

FIGURE 3-B INTERCONNECTION BLANK
3.4 USING THE BCD OUTPUTS

The BCD Outputs are buffered and gated but not stored. The transfer of output data must therefore be accomplished after a reading is completed and before it is reset.

Control input, HOLD, when high, prevents starting another conversion. If a conversion is in process when HOLD goes high, that conversion will be completed and then held. The ready signal, RDY, goes high when the data is strobed into the display (STRI pulses low) and low when the CONTROL BLOCK is reset. If HOLD is high this reset is delayed until HOLD goes low. This allows two methods of "hand shaking" data transfer. When a reading is wanted, HOLD may be taken high and when RDY goes high, the data may be printed or otherwise used after which HOLD is returned low, or RDY going high may be gated with a READ signal in the output device to generate the HOLD signal. Provided this signal is returned within 15 us, the reading will be retained while the output is used after which HOLD is returned low.

If the output device includes input storage, the trailing (rising) edge of STRI may be used to strobe this data transfer as the data will be static at that time.

The standard output gates are DTL "OR" gates (Type 1808) giving positive true outputs which are also high when disabled (DIS high). The outputs are "Collector OR able" which common bussing with other devices having this capability. Alternate IC types which are pin compatible may be substituted for these when specified on order to give inverted outputs, open collector outputs, etc. The gates are connected as follows:
4.0 CALIBRATION

4.1 INTRODUCTION

There is only one calibration control on the 6130A counter. It adjusts the frequency of the internal 1 MHz crystal controlled oscillator.

4.2 INTERNAL OSCILLATOR

The counter may be adjusted by means of the trimmer capacitor shown in the diagram. Allow at least 4 hours warm-up time before making this adjustment. The control is accessed from the side of the case. It should be adjusted with a non-metallic screwdriver. One may be made from a 1/16 inch diameter plastic rod filed to a screwdriver tip at one end. Adjust for a reading of exactly 1,000,000 Hz as read on a reference counter connected to $X_0$, Pin 9 of J1.

Adjustment at other than normal room ambient temperatures may require component changes. Consult the factory.
NOTES: DIMENSIONS IN MILLIMETERS ±0.25 MM
AND IN (INCHES) ±0.01 IN.

REAR VIEW
(TERMIAL BLOCK COVER AND BEZEL
NOT SHOWN FOR CLARITY)
CLAMP RINGS ROTATED AND SLIDE RETAINERS
REMOVED AS SHOWN FOR INSTALLATION.
06350 - CASE (REF)
(TO BE USED AS A FIXTURE
TO DETERMINE THE LENGTH
OF ITEM 76)

SPOT TIE 2 PLACES
ATTACH TO WIRE LOOPS

SHIELD E5 TO TBIB-4
RED E7 TO TBIB-5
BLACK E6 TO TBIB-6

06030-01
BOARD ASSY

.30 ± .030

REMOVE DOTTED PORTION
OF TERMINAL

VIEW A

.10 DO NOT SLEEVE
THIS AREA

DWG. NO.
06031AY-01 D